

NEWS RELEASE

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IPL Alliance Delivers Standard for Interoperable Design Constraints

IPL Constraint 1.0 Now Available to IPL members

MOUNTAIN VIEW, Calif. – June 2, 2010 – The Interoperable PDK Libraries (IPL) Alliance today announced IPL Constraints 1.0, a standard for interoperable design constraints. IPL Constraints 1.0 defines an open standard of the specifications for a set of design constraints and it is now available for validation by IPL Alliance members. IPL Constraints 1.0 will allow designers to enter constraints and design intent once and use across multiple EDA tools in their design flows, improving productivity and quality of results while reducing time to market. The IPL Alliance will present IPL Constraints 1.0 at its annual IPL Luncheon at the 48th Design Automation Conference (DAC) in San Diego California.

IPL Constraints 1.0 defines both the syntax and schema for open, interoperable design constraints. Design constraints are design-specific and distinct from foundry constraints which are based on semiconductor process design rules that are imposed by a foundry's manufacturing technology. Design constraints can be applied in many different areas including: placement, routing, timing, clock, symmetry, matching, power, floorplanning, pin, electrical, and more.

The IPL Design Constraint working group includes members from Altera, Ciranova, Pulsic, SpringSoft, Synopsys and TSMC. Additionally, Xilinx and ST Microelectronics are acting in an advisory role. The working group is now soliciting donations of additional constraints for the next version of the standard to meet emerging design challenges.

“Current analog and custom design methodologies increasingly rely on design constraints to increase productivity by improving communication among designers and enabling automation of the design process,” said Rich Morse of SpringSoft, chair of the IPL constraint working group. “There is no open standard for defining these design constraints in custom design. As a result, users are forced to enter constraints multiple times, once for each tool. To remedy this situation, the IPL Alliance has embarked on an initiative to create a single unified set of constraint definitions including both the formats and semantics of design constraints.”

The IPL Alliance will present IPL Constraint 1.0 and the latest update at the 48th Design Automation Conference (DAC) in San Diego California. An IPL Luncheon is scheduled for Monday, June 6, from 12 noon to 1:30pm at the San Diego Marriott, Marina Ballroom D-E. IPL will also be featured at the Synopsys Interoperability Breakfast on Wednesday, June 8, from 7:30am to 9:30am. The IPL Alliance demo station is located in the Synopsys Standards Booth #3328. Please visit the IPL Web site at <http://www.IPLnow.com> to register for IPL DAC events.

About the IPL Alliance

The IPL Alliance is an industry standards organization established to develop an interoperable ecosystem for custom design by creating and promoting interoperable PDK standards. There are currently 30 semiconductor and EDA company members. For more information, please visit the IPL Alliance web site at <http://www.IPLnow.com> or contact info@iplnow.com

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